MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2019/2020

ECP4256 – PRACTICAL FPGA DESIGN AND INTERFACING

(TE / RE)

29 February 2020
2.30 p.m – 4.30 p.m
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This Question paper consists of 6 pages including cover page with 5 Questions only.

2. Attempt **ALL FIVE COMPULSORY** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in the Answer Booklet provided.

Question 1

a) Explain how Static Random Access Memory (SRAM) technology could be used to implement the following programmable logic function

$$y = (a\&b)|c$$

[6 marks]

b) Give **FOUR** advantages of Field Programmable Gate Array (FPGA) over Complex Programmable Logic Device (CPLD). [4 marks]

c) The Logic Element (LE) is the smallest unit of programmable logic in Intel FPGA. Figure Q1(c) illustrates the block diagram of an LE in Intel Cyclone IV FPGA. Discuss **FIVE** features of Cyclone IV LEs. [10 marks]

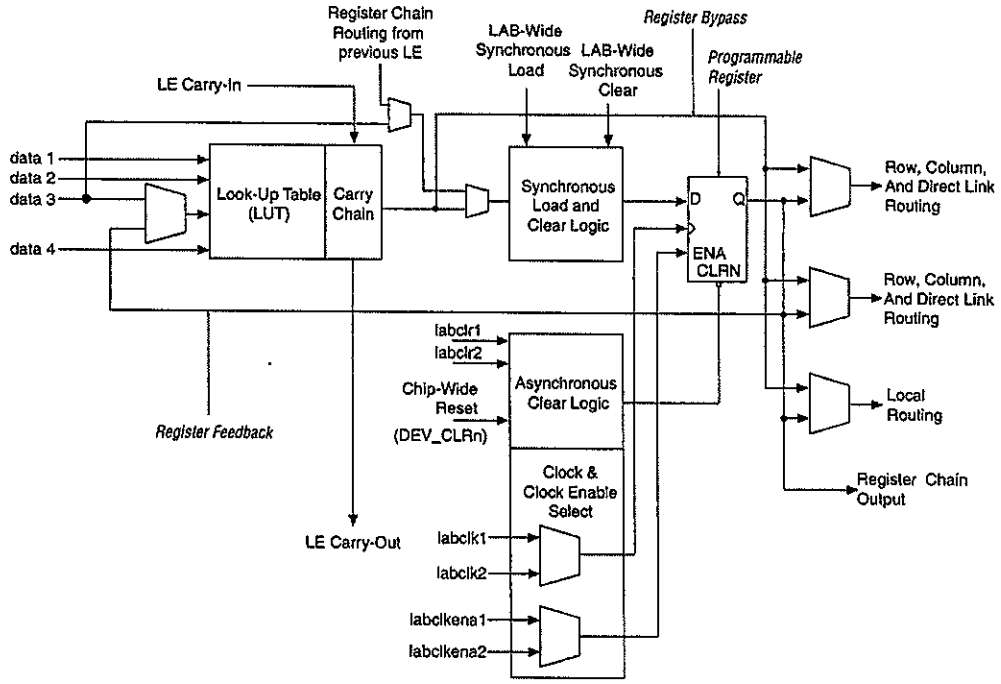

Figure Q1(c) Intel Cyclone IV Logic Element

Continued .....

Question 2

a) i) Write a complete Verilog HDL (Hardware Description Language) module to implement the following gate network. [5 marks]

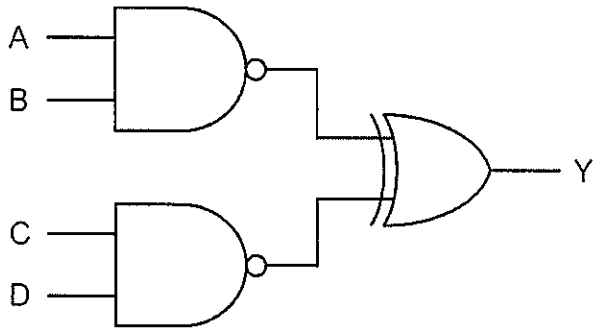

Figure Q2(a)(i)

ii) Using the module from Q2(a)(i), design a top level module as illustrated in Figure Q2(a)(ii). [6 marks]

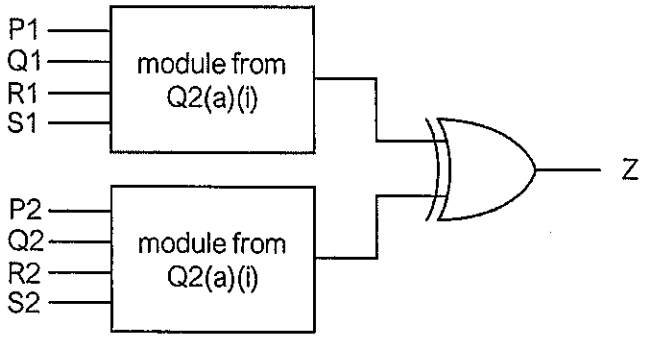

Figure Q2(a)(ii)

iii) Word size positive edge clocked binary up counter with Asynchronous Clear. [4 marks]

b) Write a testbench to verify the functionality of the logic circuit in Question 2, Part (a)(iii). [5 marks]

Continued .....

Question 3

a) What is the motivation of design optimization of a digital system? [2 mark]

b) MPEG compression standard requires an image processor to apply Discrete Cosine Transform (DCT) on the current image frame to reduce the bit-rate requirement. DCT in MPEG compression can be computed in software by performing two matrix multiplications. To decompress each picture with an image size of 720x480 pixels from the MPEG compressed video without any lagging, it requires the image processor to perform 8x8 matrix multiplication (for illuminance and chrominance blocks) at the rate of at least 4115.22 ns/block.

```
1  int CosBlock[8][8];
2
3  void MatrixMult (int a[][8], int b[][8],
4                   int c[][8]) {
5     register int i, j, k;
6
7     for (i=0; i<8; i++)
8        for (j=0; j<8; j++) {
9           c[i][j] = 0;
10          for (k=0; k<8; k++)
11             c[i][j] += a[i][k] * b[k][j];
12       }
13 }
14
15 void Transpose (int a[][8], int b[][8]) {
16    register int i, j;
17
18    for (i=0; i<8; i++)
19       for (j=0; j<8; j++)
20          b[j][i] = a[i][j];
21 }
22
```

```
23 void DCT (int InBlock[][8],
24           int OutBlock[][8]) {
25    int TempBlock[8][8], CosTrans[8][8];
26    Transpose(CosBlock, CosTrans);
27
28    /* TempBlock = InBlock * CosBlock^T */
29    MatrixMult(InBlock,CosTrans,TempBlock);
30
31    /* OutBlock = CosBlock * TempBlock */
32
   MatrixMult(CosBlock,TempBlock,OutBlock);
33 }
```

Figure Q3(b)

The sequential design of the 8x8 matrix multiplication is given in Figure Q3(b). With the aid of a diagram, explain how the following design optimization techniques could help in improving the latency of two 8x8 matrix multiplications in MPEG decompression. Also, discuss the impacts of each technique from the point of view of the execution speed of the image processor and its resource utilization in the FPGA of the optimized design.

i) Loop unrolling [6 marks]

ii) Chaining [6 marks]

iii) Multi-cycling [6 marks]

Continued .....

Question 4

a) Using the Verilog HDL kick-start code give below,

```
module PWM_generator(
  input clk,
  input en,
  input [10:0] data,
  output pulse
);

/* Your functionality design codes here */

endmodule
```

Assume that,

- A 10 MHz clock source will be connected to the `clk` input pin
- An active low enable signal will be connected to the `en` input pin
- A decimal value in the range of 0 to 1000 will be fed into the `data` input pins that will specify the pulse width of the output signal
- The period of the pulse shall be 20 ms
- The pulse width shall be in the range of 1 ms to 2 ms

Design an PWM pulse generator module using Verilog HDL to drive a servo motor. The pulse generator will output logic HIGH when the `en` pin is activated.

[8 marks]

b) Using the PWM module in part Q4(a), with the kick-start code below, design a 4-channel PWM controller. The pulse width of 1 ms will turn the servo to 0° and 2 ms will turn the servo to 180°. The angle of each servo will be specified by the `servoDataA`, `servoDataB`, `servoDataC`, and `servoDataD` input pins with the input data ranged from 0000 (0°) to 1800 (180°).

```
module PWM_Controller (
      input clk,
      input [3:0] en,
      input [10:0] servoDataA, servoDataB,
      input [10:0] servoDataC, servoDataD,
      output servoA, servoB, servoC, servoD
);

/* Your functionality design codes here */

endmodule
```

[7 marks]

c) Write a testbench to verify the functionality of your design. [5 marks]

Continued .....

Question 5

a) What is System on Chip (SoC)? Discuss **THREE** advantages of SoC implementation for a digital system. [5 marks]

b) System on a Programmable Chip (SoPC) allows the implementation of a computer and custom hardware using the available resources in an FPGA. Usually, an FPGA manufacturer will provide a "Soft" processor IP core for their FPGA fabrics (e.g., NIOS II processor for Intel FPGA and MicroBlaze processor for Xilinx FPGA). Discuss the advantages and disadvantages of a "Soft" processor on a SoPC. [5 marks]

c) Design an SoPC system on Intel Cyclone IV FPGA fabrics for a vision based smart security system with the following features,

- Read video frames from high resolution IP camera through 1000BASE-T ethernet
- Process images for human identification
- Process images for human gait identification
- Stream live output video to monitor VGA and HDMI TV
- Trigger alarm (indicator and buzzer) when suspicious human behavior is detected

* *Use a block diagram to illustrate your SoPC system design and describe the functionality of each block.*

[10 marks]

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